REMARKS

This is intended as a full and complete response to the Office Action dated April 27, 2005, having a shortened statutory period for response set to expire on July 27, 2005. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-40 are pending in the application. Claims 1-40 remain pending following entry of this response. Claims 1, 15 and 21 have been amended. Applicants submit that the amendments do not introduce new matter.

Claim Rejections - 35 USC § 112

Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Examiner states that the specification does not disclose a line propagating a DQS signal separated from a line propagating the WAIT signal.

Applicant submits, however, that the specification does disclose a line propagating a DQS signal separated from a line propagation the WAIT signal. In the specification, a single data rate (SDR) burst PSRAM with a variable latency mode is described as exemplary prior art. In variable latency mode the SDR burst PSRAM uses a WAIT Signal to indicate to the processor when a Read or Write cycle requested by the controller collides, for example, with a memory internal refresh operation, as described on page 2, paragraph [0003]. In this case, the memory asserts some number of WAIT cycles, as necessary, until completion of the refresh cycle.

To increase the data transmission speed through implementing a double data rate (DDR) concept, in contrast to a single data rate (SDR) concept, a data strobe (DQS) signal is implemented additionally to the existing WAIT signal. A possible timing diagram including such an additional DQS signal is shown in Fig. 8 (prior art). Applicant submits that one skilled in the relevant art would, for example based on Fig. 8 (prior art), conventionally implement the memory device in such a way that the WAIT signal and the DQS signal are transmitted, similar to aforementioned control signals CLK, ADV or CS over separate and individual signal lines. Thus, a conventional implementation of a

DDR burst PSRAM would increase the pin count of the memory and system controller and a width of the system bus, as described in paragraph [0007].

However, as described on page 3, paragraph [0008], an improved method and circuit configuration for implementing a double data rate feature in a memory device capable of operating in a variable latency mode is achieved by providing a bi-directional line to transmit a signal that comprises the combined functionality of a WAIT signal and a data strobe (DQS) signal, therefore referred to as the WAIT_DQS signal. The advantage of the invention is a reduced number of required pins and reduced bus width (by replacing a line used for propagating a conventional WAIT signal or a line used for propagating a conventional DQS signal).

Claim Rejections - 35 USC § 103

Claims 1-2, 5-9 and 11-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Lee* (PGPub. 2004/0022095) in view of *Nystuen et al.* (U.S. Patent No. 6,603,706, referring hereinafter as *Nystuen*).

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the third criterion.

For example, Applicant submits that the cited references, alone or in combination, do not teach a method, device, or system utilizing a WAIT_DQS signal propagated on a bi-directional line that combines functionality of a data strobe signal and a wait signal and "has a WAIT state until completion of a refresh operation, in the event that a read cycle collides with an execution of the refresh operation", as claimed in independent claims 1, 15, and 21.

While the Examiner refers to strobe signals *SDtM* and *SDfM* taught in *Lee* as performing the same functionality as the claimed WAIT_DQS signal, the Examiner

concedes *Lee* does not teach propagating these signals on a single bi-directional line. The Examiner cites *Nystuen* as teaching a bi-directional *DQS* line and asserts it would have been obvious to one skilled in the art to use a bi-directional line as taught in *Nystuen* to transmit the strobe signals *SDtM* and *SDfM* of *Lee*. However, Applicant submits the *SDtM* and *SDfM* of *Lee* do not perform the same functionality as the claimed WAIT_DQS signal, even if propagated on a single bi-directional line.

In contrast, the strobe signal *SDtM* is used to read data from the memory array and latch it (see paragraph [0032] of *Lee*), while the *SDfM* strobe signal is used to transmit (in a second step) data already read out from memory and stored in a buffer or latch to the controller. Neither of these signals performs the claimed functionality of a WAIT signal, such as "indicating when valid data is present on the data bus during a read cycle and when the memory device is ready to accept data during a write cycle."

Furthermore, the above-referenced signals in *Lee* do not perform WAIT functionality by adding additional wait cycles due to an ongoing refresh operation, as claimed. On the contrary, *Lee* discloses that a strobe generation circuit generating the strobe signal SDfM "delays the second strobe signal SDtM a delay time associated with operation of a latch to generate the third strobe signal SDfM" and "the strobe generation circuit being, for example, a delay line, phase or delay lock loops, and oscillator or other such strobe generation circuits known to those skilled in the art". See paragraph [0033]. In other words, *Lee* discloses a *fixed* latency between the second and the third strobe, which is in complete contradiction to the WAIT functionality described in the independent claims, whereby the memory can add additional WAIT cycles to finish an ongoing refresh operation, before reading out any data from the memory.

For these reasons, Applicant submits claims 1, 15, and 21, as well as their dependents, are in condition for allowance, and allowance of these claims is respectfully requested.

Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Lee* in view of *Nystuen* further in view *Kuge* (U.S. Patent No. 6,466,496).

Kuge fails to overcome the deficiencies in the teachings of *Lee* and *Nystuen* as described above, with respect to independent claims 1 and 21. Accordingly, because

claims 3 and 22 depend from claims 1 and 21, these claims are also believed to be in condition for allowance, and allowance of the claims is respectfully requested.

Therefore, the claims are believed to be in condition for allowance, and allowance of the claims is respectfully requested.

Claims 4, 10 and 23-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Lee* in view of *Nystuen* further in view *Jakobs* (PGPub. 2004/0047227).

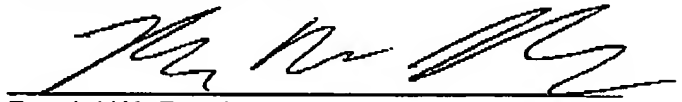
Jakobs fails to overcome the deficiencies in the teachings of *Lee* and *Nystuen* described above, with respect to independent claims 1 and 21. Accordingly, because claims 4, 10 and 23-40 depend from claims 1 and 21, these claims are also believed to be in condition for allowance, and allowance of the claims is respectfully requested.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted,



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